Heavy Ion SEE Tests of Texas Instruments 65 nm CMOS SRAMs

Mike Xapsos and Ken LaBel, Code 561, NASA/GSFC
Hak Kim, Mark Friendlich, Anthony Phan,
Michael Campola and Chris Seidleck MEI Technology
Alan Tipton, John Hutson, Jonathan Pellish and Robert Reed, Vanderbilt University
Xiaowei Deng, Andrew Marshall and Robert Baumann, Texas Instruments

I. Introduction

This testing was undertaken to study angular effects for Single Event Upset (SEU), Multiple Bit Upset (MBU) and Single Event Latch-up (SEL) in 65 nm CMOS SRAMs. The test chips were fabricated by Texas Instruments (TI).

II. Devices Tested

The SRAMs were bonded directly to test boards at Radiation Assured Devices in Colorado Springs, CO using a layout designed at GSFC. The identification information for these SRAMs according to TI is:

Test Chip: x1886

Lot # 4071614

Wafer # 7

Module: T21YR8M

The device technology is 65 nm CMOS. There are 8 memory sections consisting of 1 Mbit each. Two sections are high performance (HP), which consist of the largest size transistors. The remaining 6 sections consist of smaller transistors for high density applications. There are two types of high density memory sections, two Mbits of type HD-B and 4 Mbits of type HD-POR.

III. Test Facility and Ions

Facility: Texas A&M Cyclotron Facility

Ions: The following table shows the ions used and relevant characteristics.

Ion:	Primary Energy (MeV/u):	Energy at SRAM Surface (MeV/u)*:	LET (MeV-cm^2/mg)*:	Range (μm)*:
Ne	15	13.5	2.8	266
Ar	15	12.6	8.6	179
Cu	15	11.5	20.4	122
Kr	15	11.3	28.9	121

*Accounts for beam line exit window and 52 mm air gap

Flux: Fluxes were approximately 10^2 ions/cm^2/s for SEU/MBU tests. They were in the range of 10^2 to 10^5 ions/cm^2/s for SEL tests.

Fluence: SEU/MBU tests were run to acquire sufficient statistics during an irradiation. In order to ensure that MBU were due to single ions the number of upset bits per irradiation was kept under 800. This is 4 orders of magnitude less than the total number of bits in the memory.

SEL irradiations were continued until either latch-up was observed or a fluence of 10^7 ions/cm^2/s was reached. SEL was assumed to occur if a current twice the magnitude of the stand-by current was observed during irradiation.

IV. Test Conditions

Test Temperature: Room temperature (22 C) for SEU/MBU tests and room temperature to 80 C for SEL tests

Operating Frequency: Static

Power Supply Voltage: V_{dd} = 1.2 V
n-well bias (VNWA) = 0.5 V for SEU/MBU tests and 1.8 V for SEL tests

Test Pattern: Logical checkerboard for SEU/MBU tests

Monitoring TID: Supply (leakage) current I_{dd} was measured after each irradiation to monitor parametric degradation from TID. No significant change was observed during testing.

Angular Data: Data were taken with ions normally incident on the test chips and with the test boards rotated by 45 and 79 degrees relative to the beam for 2 different board orientations. From a macroscopic view the chip is laid out with alternating columns of n-wells and p-wells. For large angles of incidence the 2 board orientations result in ions that are incident along the wells and across (against) the wells.

The test set-up is shown in Figure 1.

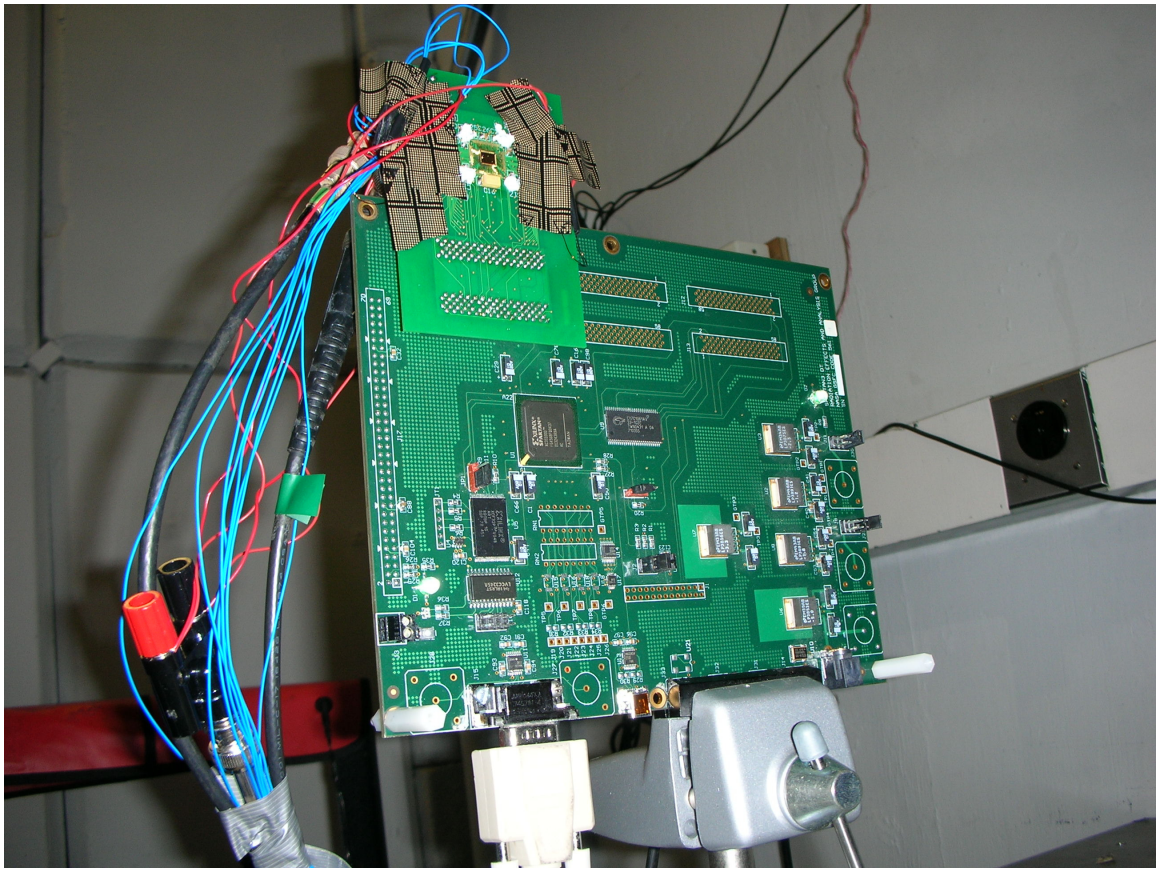

Figure 1. Test set-up used for SEE testing at the Texas A & M cyclotron facility.

V. Results

A. SEU/MBU Cross Sections

Figures 2 and 3 show the single-bit upset (SBU) cross sections and the MBU cross sections, respectively. Results are shown for normally incident ions and for ions incident at 45 and 79 degrees for the 2 different board orientations.

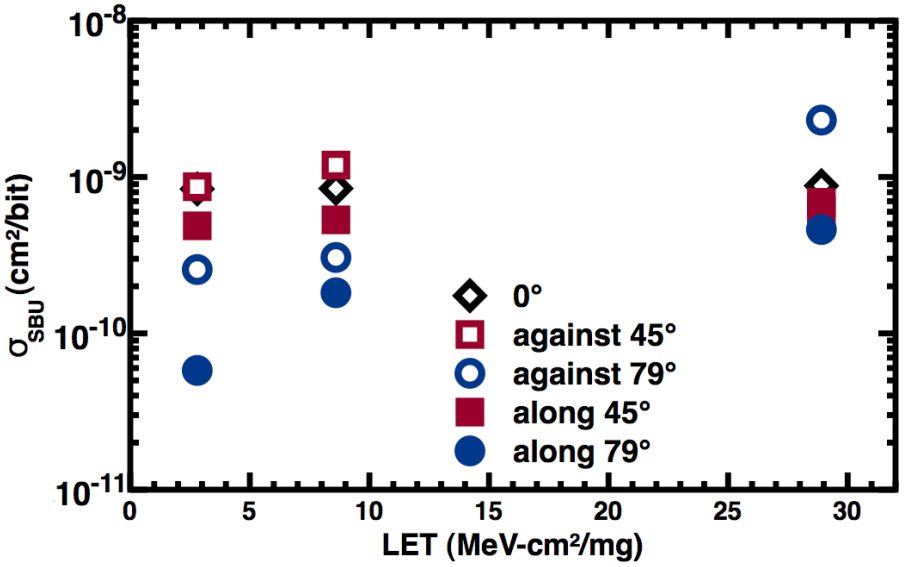

Figure 2. Single-bit upset cross sections as a function of ion LET, angle of incidence and board orientation. For large angles of incidence the 2 board orientations correspond to ions incident along the n- and p-wells and across (against) the n- and p-wells.

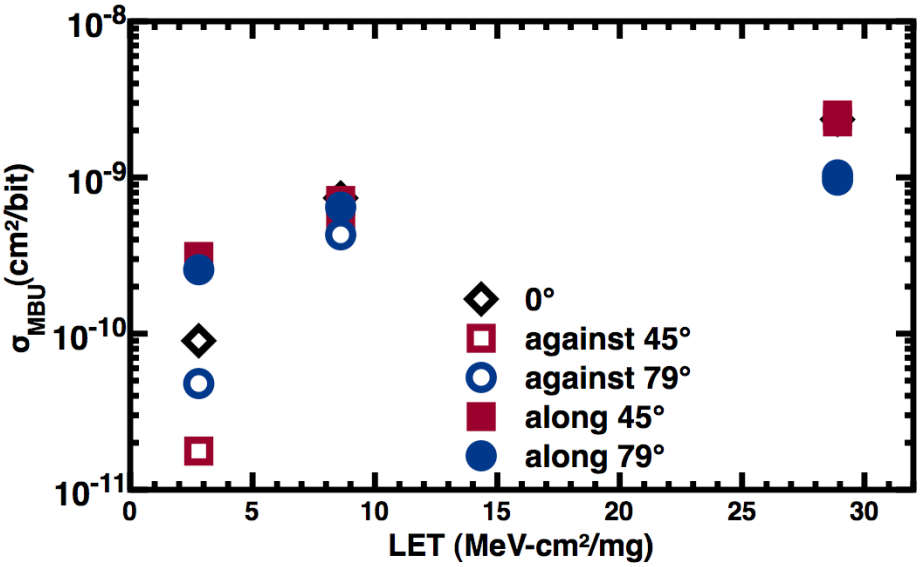

Figure 3. MBU cross sections as a function of ion LET, angle of incidence and board orientation. For large angles of incidence the 2 board orientations correspond to ions incident along the n- and p-wells and across (against) the n- and p-wells.

B. SEL Temperature Thresholds

Figure 4 shows results for the threshold temperature for SEL for both normally incident ions and for ions incident at a 79 degree grazing angle for both board orientations.

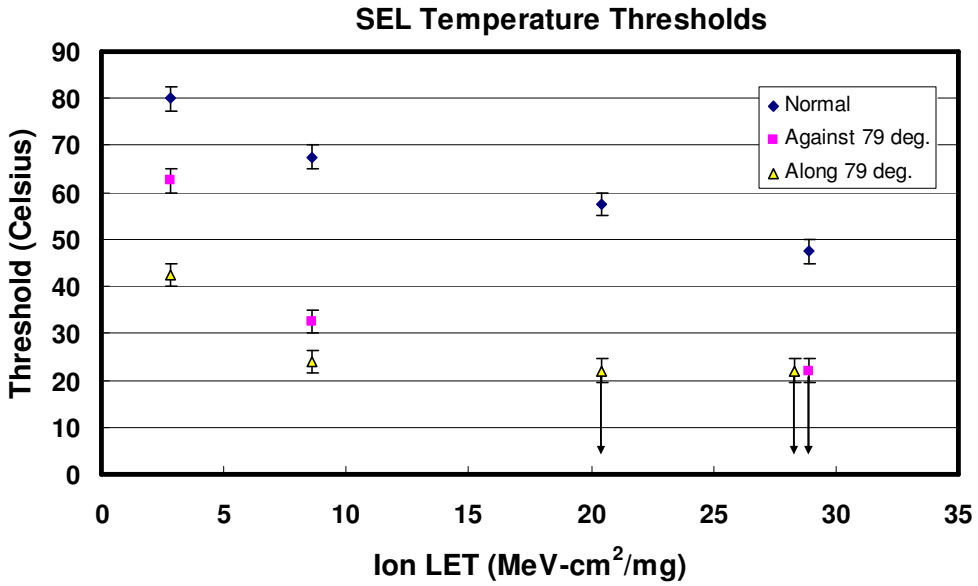

Figure 4. Threshold temperature for SEL as a function of ion LET, angle of incidence and board orientation. For large angles of incidence the 2 board orientations correspond to ions incident along the n- and p-wells and across (against) the n- and p-wells. The downward pointing arrows indicate no lower limit was determined because the SRAMs experienced latch-up at room temperature.

VI. Summary

We have presented heavy ion test results for SEU, MBU and SEL in TI 65 nm CMOS SRAMs. All measured effects are dependent on not only the incident ion LET and angle of incidence, but also the orientation of the test board. These results have been further analyzed in [1], [2].

[1] A.D. Tipton et al., "Device-Orientation Effects on Multiple-Bit Upset in 65-nm SRAMs", IEEE Trans. Nucl. Sci., Vol. 55, Dec. 2008 (accepted for publication).
[2] J.M. Hutson et al., "Analysis of Single-Event Latchup Cross Section in 65 nm SRAMs", IEEE Trans. Nucl. Sci., Vol. 55, Dec. 2008 (accepted for publication).